MAGNETIC RANDOM ACCESS MEMORY DEVICE CAPABLE OF PROVIDING A CONSTANT CURRENT TO A REFERENCE CELL

Field of the Invention

The present invention relates to a magnetic random access memory device and, more particularly, to a magnetic random access memory device capable of providing a constant current to a reference cell.

Background of the Invention

A magnetic random access memory ("MRAM") device is a kind of a non-volatile memory device, which includes a plurality of magnetic memory cells. MRAM uses magnetic charges to store bits of data. In general, the structure of an MRAM device includes, memory cells having non-magnetic film and magnetic film alternately stacked. For example, a memory cell of an MRAM device may include an insulating film interposed between two magnetic films. The memory cell is written by changing the magnetization direction (i.e., polarity) of one of the magnetic films. The change in polarity results in a considerable change in resistance, which is known as the giant magnetoresistive effect ("GMR"). The overall resistance of the magnetic memory cell has a maximum value or a minimum value according to magnetization directions of the magnetic film. For example, if the magnetic directions of the magnetic films are identical with each other, (i.e., a "parallel"

state), an overall resistance is relatively low. In the parallel state, the memory cell is clear (e.g. "0") and considered to be in a logic low ("L") state. In contrast, if the magnetic directions are adverse to each other, (i.e., an "anti-parallel" state), an overall resistance is relatively high. In the anti-parallel state, the memory cell is holding data (e.g. "1") and considered to be in a logic high ("H") state.

To read the logic state of a magnetic memory cell, the MRAM device applies a sense current and a reference current to a target cell and a reference cell, respectively. A voltage drop occurs at both ends of the target cell and the reference cell depending on the respective resistance values of the cells. The voltages of the cells are compared with each other to determine a logic state of the target cell. FIG. 1 shows a conventional 32Kb MRAM memory block including a midpoint reference generator therein. FIG. 1 originates from FIG. 7 of a paper reporting the demonstration of MRAM from the 2002 VLSI Symposiaon Technology and Circuits.

Referring to FIG. 1, the midpoint reference generator has four magnetic resistors that are connected in series and parallel. A serially-connected resistor is connected to another serially-connected resistor in parallel resulting in a resistor having a value equal to (Rmax+Rmin)/2. The resistance (Rmax+Rmin)/2 represents a reference resistance that is halfway between the value of a resistance in a logic low (L) state and a logic high (H) state. A problem exists in that the resistance of the midpoint reference generator varies with the level of a bitline clamp voltage (reference voltage) Vref.

Referring to FIG. 2, a difference between a maximum resistor value Rmax and a minimum resistor value Rmin, when the bitline clamp voltage Vref is equal to a set value, is less than a difference therebetween when the bitline clamp voltage Vref is less than the set value. That is, when the level of the bitline clamp voltage Vref is high, a value of the resistor (Rmax+Rmin)/2 is low. In contrast, when the level of the bitline clamp voltage Vref is low, the value of the resistor (Rmax+Rmin)/2 is high. Accordingly, the midpoint reference generator must control the bitline clamp voltage Vref to maintain the desired value of the resistor (Rmax+Rmin)/2. However, the desired bitline clamp voltage can be attained only by trial and error. Further, restructuring of a bitline clamp voltage of the reference cell is considerably troublesome. Therefore, in order to precisely compare a target cell with a reference cell, there is a need for an MRAM device that produces a constant reference output regardless of changes in bitline clamp voltage.

Summary of the Invention

In view of the foregoing, a memory device, in accordance with the present invention outputs a constant reference current to a reference cell irrespective of a bitline clamp voltage.

A memory device, in accordance with the present invention, includes a first memory array having a plurality of memory cells, wherein each one of the plurality of first memory cells is arranged at an intersection of at least one of a plurality of wordlines, at least one of a plurality of bitlines, and at least one of

a plurality of digit lines, a second memory array having a plurality of second memory cells, wherein each one of the plurality of second memory cells is arranged at an intersection of at least one of the plurality of wordlines, at least one of a first bitline and a second bitline, and at least one of the plurality of digit lines, a current providing unit for providing a second current to one of the first bitline and the second bitline in response to a reference voltage, and a sense amplifier for comparing a first current flowing through one of the plurality of bitlines with the second current.

In alternate embodiments, a current providing unit may include a first current mirror coupled to the first bitline, wherein a current from the first bitline flows through the first current mirror in response to the reference voltage, a second current mirror coupled to the second bitline, wherein a current from the second bitline flows through the second current mirror in response to the reference voltage, and a third current mirror for providing half of the sum of the current from the first bitline and the current from the second bitline to the sense amplifier. Each one of the plurality of second memory cells may be set to a first logic state and coupled to the first bitline or set to a second logic state and coupled to the second bitline. The memory device may further include a clamp circuit for clamping down a voltage of a data line through which the first current is transmitted, and a voltage of a data line through which the second current is transmitted, to the reference voltage when one of the plurality of wordlines of one of the plurality of first memory cells is enabled. The first memory cells and the second memory cells may be

magnetic. The second current may be a reference current defined by the expression (i(H)+i(L))/2. The first current may be a target current. The first current may be compared to the second current to determine a logic state of a predetermined one of the plurality of first memory cells.

Another memory device, in accordance with the present invention, includes a plurality of first bitlines and a plurality of second bitlines, a first memory array having a plurality of first memory cells, a second memory array having a plurality of second memory cells, a current providing unit for providing a second current to one of the plurality of second bitlines in response to a reference voltage, and a sense amplifier for comparing a first current flowing through one of the plurality of first bitlines with the second current.

In alternate embodiments, the current providing unit may include a first current mirror coupled to a first one of the plurality of second bitlines, a second current mirror coupled to a second one of the plurality of second bitlines, and a third current mirror for providing half of the sum of a current from the first current mirror and a current from the second current mirror to the sense amplifier. Each one of the plurality of second memory cells may be set to a first logic state and coupled to a first one of the plurality of second bitlines or set to a second logic state and coupled to a second one of the plurality of second bitlines. The memory device may further include a circuit for clamping down a voltage of a line through which the first current is transmitted, and a voltage of a line through which the second current is

transmitted, to the reference voltage. The first memory cells and the second memory cells may be magnetic. The second current may be a reference current defined by the expression (i(H)+i(L))/2. The first current may be a target current. The first current may be compared to the second current to determine a logic state of a predetermined one of the plurality of first memory cells.

Brief Description of the Drawings

Preferred embodiments of the invention can be understood in more detail from the following descriptions taken in conjunction with the accompanying drawings in which:

FIG. 1 shows a conventional MRAM device;

FIG. 2 shows variations in reference resistance based on bitline clamp voltage of the midpoint reference generator shown in FIG. 1;

FIG. 3 shows an MRAM device according to an embodiment of the present invention;

FIG. 4 shows a reference current providing unit of the MRAM device shown in FIG. 3; and

FIG. 5 shows a bitline clamp circuit of the MRAM device shown in FIG. 3.

Detailed Description of Preferred Embodiments

Preferred embodiments of the present invention will now be described

more fully hereinafter below in more detail with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention may, however, be embodied in different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. Like numerals refer to like elements throughout the specification.

An MRAM according to the present invention is now described below with reference to FIG. 3.

Referring to FIG. 3, an MRAM 300 includes a memory array block 310, a reference memory array block 320, a wordline selecting unit 330, a digit line selecting unit 340, a bitline/reference bitline selecting unit 350, a reference current providing unit 360, a bitline clamp circuit 370, and a sense amplifier (S/A) 380. The memory cell array block 310 has magnetic memory cells arranged at intersections of wordlines WL0, WL1, WL2, and WL3 (collectively referred to as "WL"), bitlines BL0, BL1, BL2, and BL3 (collectively referred to as "BL"), and digit lines DL0, DL1, DL2, and DL3 (collectively referred to as "DL"). Magnetic memory cells coupled to a first reference bitline RBL0 are set to a logic high ("H") state, and magnetic memory cells coupled to a second reference bitline RBL1 are set to a logic low ("L") state.

The wordline selecting unit 330 selects one of the wordlines WL, and the bitline selecting unit 350 selects one of the bitlines BL for targeting a cell to be read. Similarly, the digit line selecting unit 340 selects one of the digit

lines DL and determines the direction of digit current (ID).

The reference current providing unit 360 is explained in detail with reference to FIG. 4.

Referring to FIG. 4, the reference current providing unit 360 has first to third current mirrors 363, 366, and 369 connected with first and second reference bitlines RBL0 and RBL1 of the reference memory array block 320. A current mirror is a circuit that can produce an output current that mirrors an input current. The output current may remain constant regardless of an actual voltage.

A first current mirror 363 is coupled to the first reference bitline RBL0. Current i(H) flows to a first transistor 361 of the first current mirror 363 in response to a predetermined bitline clamp voltage VREF, enabling the current i(H) to flow to a second transistor 362. Channel width and length of the first and second transistors 361 and 362 are equal to each other. The second current mirror 366 is coupled to the second reference bitline RBL1. Current i(L) flows to a third transistor 364 in response to the predetermined bitline clamp voltage VREF, enabling the current i(L) to flow to a fourth transistor 365. Channel width and length of the third and fourth transistors 364 and 365 are equal to each other. Current i(H)+i(L) equals the sum current of the current i(H) provided from the second transistor 362 and the current i(L) provided from the fourth transistor 365. The current i(H)+i(L) flows to a fifth transistor 367 of the third current mirror 369. A sixth transistor 368 is set to have half the channel length of the fifth transistor 367, so that current (i(H)+i(L))/2 flows to

the sixth transistor 368. Referring to FIG. 5,the current (i(H)+i(L))/2 flowing in the reference current providing unit 360 flows to a reference data line through a reference bitline RBL. Bitline clamp current (iT) provided from the bitline clamp circuit 370 also flows to the reference data line. Thus, current iT-(i(H)+i(L))/2 flows through the reference data line and the reference data line is coupled to a sense amplifier 380. A magnetic memory cell selected in the memory array block 310 is coupled to a data line through a bitline BL. At this time, current flowing through the bitline BL is the current i(H) or i(L) according to a logic state of the selected memory cell. The bitline clamp current (iT) provided from the bitline clamp circuit 370 also flows to the data line, enabling current iT-i(H) or iT-i(L) to flow through the data line.

The sense amplifier 380 senses and amplifies the current flowing through the data line and the reference data line to determine the logic state of the selected magnetic memory cell. While current iT-(i(H)+i(L))/2 flows through the reference data line, the bitline clamp voltage VREF must be high enough to turn on the first to fourth transistors 361, 362, 364, and 365 in the first and second current mirrors 363 and 366. Although the bitline clamp voltage VREF is varied to surpass the transistor turn-on levels, currents flowing through the reference bitline and the reference data line remain constant (i.e., (i(H)+i(L))/2 and iT-(i(H)+i(L))/2, respectively) regardless of the variation of the bitline clamp voltage.

The bitline clamp circuit 370 is coupled between a data line and a reference data line and the sense amplifier (S/A) 380 and includes differential

amplifiers 372 and 374, a driving unit 376, and a current providing unit 378. The differential amplifier 372 receives a data line voltage to control the driving unit 376 such that the data line voltage is equivalent to the bitline clamp voltage VREF. This allows the data line and the reference data line, which are precharged to an earth line or ground when a wordline is enabled, to rise up to a voltage level equal to the bitline clamp voltage VREF.

According to the data value of the selected memory cell, current i(H) or i(L) flows to the data lineIn addition, constant current iT-(i(H)+i(L))/2 flows to the reference data line without a requiring adjustment to the level of the bitline clamp voltage VREF. As a result, the operation of a sense amplifier 380 of comparing the current iT-i(H) or iT-i(L) of the data line to the current iT-(i(H)+i(L))/2 of the reference data line is more stable and efficient.

Although the illustrative embodiments have been described herein with reference to the accompanying drawings, it is to be understood that the present invention is not limited to these precise embodiments, and that various other changes and modifications may be affected therein by one of ordinary skill in the related art without departing from the scope or spirit of the invention. All such changes and modifications are intended to be included within the scope of the invention as defined by the appended claims.